REMARKS

1. Amendments to Specification and Drawings

Fig. 1 is replaced by Figs. 1(a) and 1(b), both labeled –(PRIOR ART)–. Figs. 1(a) and 1(b) show the prior art in greater detail so that the distinguishing features of the present invention can be better understood.

In particular, replacement Figs. 1(a) and 1(b) show the manner in which the FET 1 is shunt connected between the signal lines 2 and 3, with Fig. 1(b) showing how the prior art (*i.e.*, the Nakahara patent) uses a parallel-connected inductor 8 to compensate for the parasitic drain-to-source capacitance of the FET when the switch is used at high frequencies. This is in contrast to the present invention, which uses an impedance transformation network rather than a parallel-connected inductor in order to improve the isolation performance of the FET.

Figs. 2 and 4 have also been amended to more clearly show the connections between the various transmission lines, which were confusingly depicted in the original drawings. In addition, reference numerals have been added to both Figs. 2 and 4. Fig.3 is unchanged.

Because new Fig. 1(b) shows a well-known prior art circuit configuration, and is clearly labeled as prior art, it is respectfully submitted that the addition of new Fig. 1(b) does not involve **new matter**. In addition, because the changes to the Figs. 1(a), 2 and 4 merely involve labeling and the style in which the connections between the transmission lines and FET are schematically depicted, without adding any new elements, it is respectfully submitted that the changes to Figs. 1(a), 2, and 4 do not involve **new matter**.

2. Objection to Claims

This objection has been addressed by amending claim 3 to be in proper alternative-dependence format.

3. Rejection of Claims 1 and 2 Under 35 USC §102(b) in view of U.S. Patent No. 5,485,130 (Nakahara)

This rejection is respectfully traversed on the grounds that the Nakahara patent fails to disclose or suggest an **impedance transformation network** connected in **series** with the drain and source of the FET, and then connected with the signal line, as recited in claim 1. Instead, the Nakahara patent discloses an FET with an **inductor** connected in **parallel** with the drain and source of the FET. While an "impedance transformation network" could read on an inductor, the claimed "impedance transformation network" cannot possibly read on the inductor of Nakahara since the inductor of Nakahara is connected in parallel and not in series with the FET.

Although the term "series-connected" should be sufficient to distinguish the claimed invention from the parallel-inductor arrangement of Nakahara, it is noted that claim 1 has been amended to positively recite the absence of a parallel-connected "reactance component" such as an inductor, thereby even more clearly distinguishing the Nakahara patent.

The main objective of the Nakahara device is to replace the two 50-Ohm transmission lines of the conventional FET switch design by a pair of high and low impedance transmission lines 4a and 4b, shown in Fig. 1 of Nakamura. This has the effect of improving the power transmission efficiency via an impedance transformation. However, this requires use of the parallel-connected inductors. In contrast, the claimed invention simply adds an impedance transformation network (which may be in the form of three transmission lines 4, 5, and 6, **in series** with the FET to achieve a near short circuit when the FET is switched OFF and a near open circuit when the FET is switched ON, thereby significantly improving isolation.

The following Smith Charts, labeled Fig. A, Fig. B, and Fig. C illustrate the differences in operation between the prior art device of Fig. 1(a), the device of Nakahara, and the claimed device:

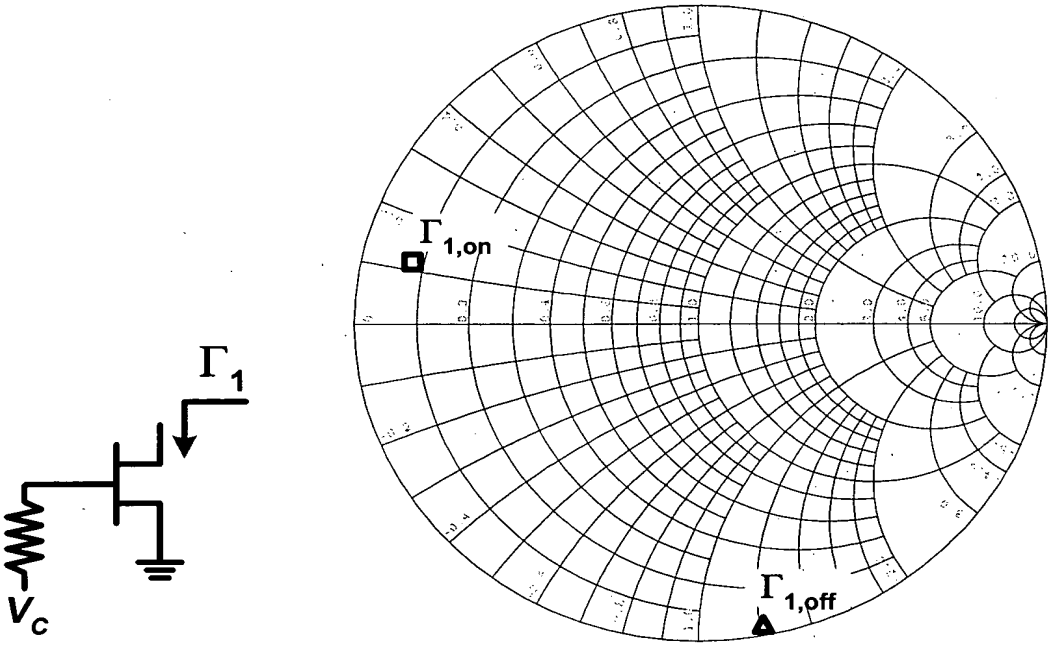

Fig. A. On- and off-state input impedances of a shunt FET.

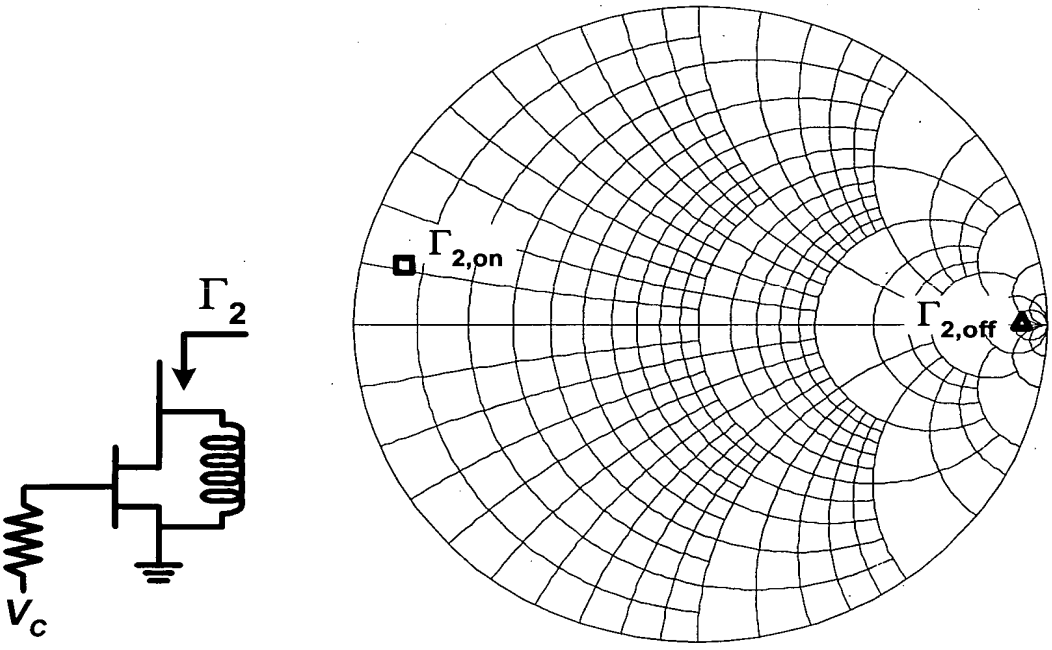

Fig. B. On- and off-state input impedances of a shunt FET with a resonant inductor.

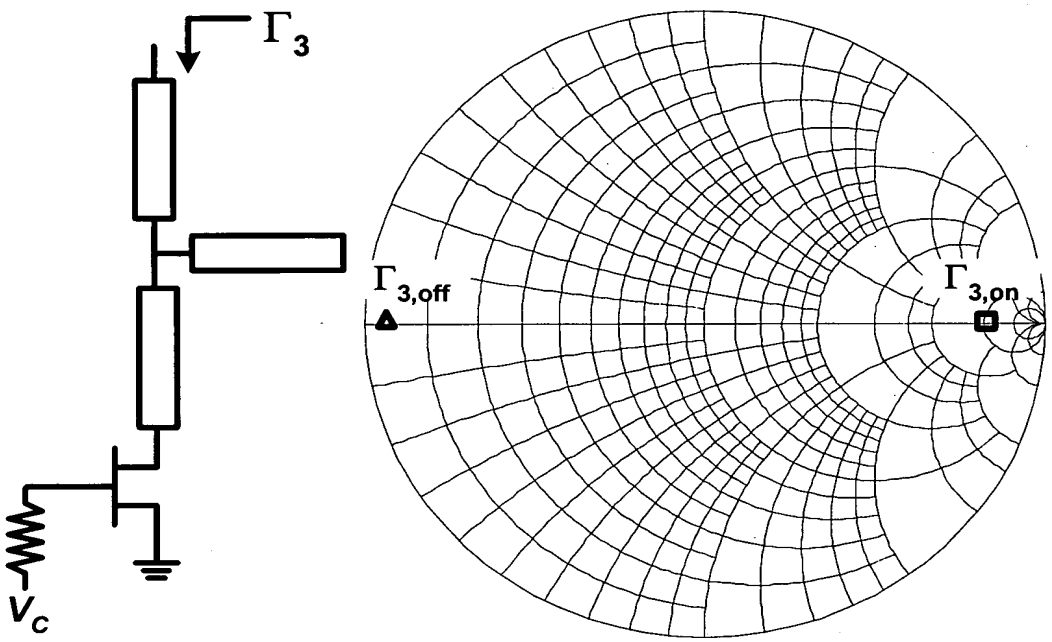

Fig. C. On- and off-state input impedances of a shunt FET with the impedance transformation network.

The Nakahara patent, with its parallel inductors 8a and 8b, basically shows the circuit illustrated in prior art Fig. 1(b), corresponding to the Smith Chart of Fig. B, above. There are clearly no series-connected impedance transformation networks connected between the FETs 7a and 7b, and the signal lines 4a, 4b, and 5 of Nakahara. In such a parallel-inductor circuit,), the off-state is ideal, but the on-state is not. The reason is that the impedance of the on-state FET remains low despite the inductor, and even though the inductor resonates the off-state impedance of the FET to provide a high impedance.

Of course, the arrangement of Nakahara is better than the arrangement illustrated in Fig. 1(a), corresponding to the Smith Chart of Fig. A, above, which has no impedance compensation and therefore has poor on and off states. However, it is clearly inferior to the claimed FET with series-connected impedance transformation network, which corresponds to the Smith Chart of Fig. C, and which has ideal on and off states. By using the series-connected impedance transformation network of the invention, the invention transforms on- and off- state impedances to near open and near short.

These differences are summarized in the following table:

Features	**Nakahara**	**Claimed**	Comparison
Compensation method for FET	Parallel inductor to resonate off-state capacitor of the off-state FET	Series-Connected Impedance transformation network to transform on- and off-state impedances to near open and near high simultaneously (no parallel inductor or other reactance component)	Parasitic Impedances Such as Via hole inductance could be fully compensated by using impedance transformation network-not possible with parallel inductor of Nakahara
Input impedance of the FET with compensation	ON state: low impedance OFF state: high impedance	ON state: high impedance OFF state: low impedance	Nakahara: on-state impedance has reactance Claimed: both of on- and off-state impedance have no reactance

Purpose of 50-Ω quarter-wavelength transformer	transform low impedance to high impedance (conventional design)	transform low impedance to high impedance (conventional design)	
Purpose of low-impedance quarter-wavelength transformer	transform low impedance to high impedance, improve the power handling performance of the switch	not use low-impedance transformer	Low impedance transformer in Nakahara is used to improve the performance of the switch

Because the Nakahara patent fails to disclose or suggest the positively recited feature of a series-connected impedance transformation network, much less one without any parallel reactance connected between the source and drain of the FET, and because this feature withdrawal of the rejection of claims 1 and 2 under 35 USC §102(b) is respectfully requested.

Having thus overcome each of the rejections made in the Official Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

Respectfully submitted,

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Date: July 11, 2003

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